



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Chen *et al.*

Appl. No.: 10/643,957

Filed: August 20, 2003

For: **High Voltage Power Management  
Unit Architecture in CMOS Process**

Confirmation No.: 4983

Art Unit: 2838

Examiner: Patel, Rajnikant B.

Atty. Docket: 1875.4170000/JTH/GSB

**Declaration of Chun-Ying Chen and Hsiang-bin Lee  
Under 37 C.F.R. § 1.131**

Commissioner for Patents  
PO Box 1450  
Alexandria, VA 22313-1450

Sir:

The undersigned, Chun-Ying Chen and Hsiang-bin Lee, declare and state that,

1. We are the inventors of the above-captioned application, U.S. Appl. No. 10/643,957, filed August 20, 2003.

2. Prior to July 10, 2003, we, the inventors, had completed our invention in the United States, as claimed in the subject application, evidenced by the following:

3. Invention disclosure, attached as Exhibit A, which confirms the conception date at least as early as February 27, 2003 (see page 2 of the Exhibit).

4. Email dated July 10, 2003 forwarding first draft of the application, attached as Exhibit B, showing work on constructive reduction to practice.

5. Thus, the invention was conceived prior to the earliest filing date of Yang et al., U.S. Patent No. 6,765,374, and the inventors and their patent attorneys were working diligently on constructive reduction to practice between the filing date of Yang et al. and August 20, 2003, the filing date of this application, as also shown in the Declaration under 37 C.F.R. § 1.131 by George S. Bardmesser and the exhibits attached thereto.

6. As the persons signing below, we hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under § 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issue thereupon.

2/18/2005  
Date

Chun-Ying Chen

2/18/05  
Date

Hsiang-bin Lee



# BROADCOM CORPORATION

**CONFIDENTIAL**

Forward to:  
Dee Henderson  
Intellectual Property Coordinator  
Ext. 5958, dhen@broadcom.com

Broadcom File No. BP2864

Date: \_\_\_\_\_

BCM Chip No. \_\_\_\_\_

## INVENTION DISCLOSURE FORM

SK

1. Title of Invention High Voltage Power Management Unit Architecture in CMOS Process

Inventor(s) Chun-Ying Chen  
Full Name  
15 Ashford  
Residence Address  
Irvine, CA 92618  
City, State, Zip  
USA  
Citizenship

Hsiang-bin Lee  
Full Name  
116 Las Flores  
Residence Address  
Aliso Viejo, CA 92656  
City, State, Zip  
Taiwan  
Citizenship

Inventor(s)  
Full Name  
Residence Address  
City, State, Zip  
Citizenship

Full Name  
Residence Address  
City, State, Zip  
Citizenship

Inventor(s)  
Full Name  
Residence Address  
City, State, Zip  
Citizenship

Full Name  
Residence Address  
City, State, Zip  
Citizenship

Inventor(s)  
Full Name  
Residence Address  
City, State, Zip  
Citizenship

Full Name  
Residence Address  
City, State, Zip  
Citizenship

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Invention Disclosure Form (*cont'd*)

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2. When was the invention first conceived? Oct 11, 2002
3. (a) When were first sketches, diagrams or drawings made? Oct 11 2002  
(Append copies.)  
(b) Where are they? Broadcom, Irvine  
(c) Drawing or Notebook Ref. Nos. \_\_\_\_\_
4. (a) When was first written description made? Oct 11, 2002  
(Append copy.)  
(b) Where is it? Broadcom, Irvine
5. (a) When was first explanation of invention made to others? Oct 11, 2002  
(b) Where? Broadcom, Irvine  
(c) To whom? Todd Brook
6. (a) When was model of invention first built? Dec 1, 2002  
(b) Where? Broadcom, Irvine
7. (a) When was model of invention first tested or demonstrated? Feb 24, 2003  
(b) Where? A2003 Broadcom, Irvine  
(c) Present location of model tested Broadcom  
(Append photographs.)  
(d) Who witnessed such test or demonstration? Tood Brook, Venu Gopinathan
8. Has the invention been (a) publicly disclosed; (b) placed in commercial use; (c) offered for sale or sold; or (d) described in a printed publication?  Yes       No

If "Yes," describe the first occurrence of each of (a) through (d), respectively, and give dates, places and identification.

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If "no," are any of (a) through (d) contemplated?  Yes       No

9. Identify known closely related publications, patents and patent applications and prior products.

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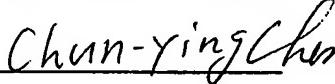
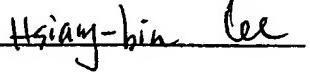
# BROADCOM CORPORATION

Invention Disclosure Form (*cont'd*)

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SIGNATURES: Please sign and date. Print name below signature line.

Signature of inventor(s)

	Date <u>2/27/03</u>
	Date _____
	Date <u>2/27/03</u>
	Date _____
_____	
_____	

## INSTRUCTIONS FOR SUBMISSION AND APPROVAL:

1. Submit original to Dee Henderson
2. Forward one copy to Engineering Manager for approval and circulation to Engineering Director/VP and Business Unit VP/GM. (Print name below signature line.)
3. Business Unit VP/GM will forward approved copy to Dee Henderson

## ENGINEERING MANAGER APPROVAL: (required, if applicable)

	Date <u>2/27/2003</u>
(print name) _____	
COMMENTS: _____	

## ENGINEERING DIRECTOR/VP APPROVAL: (required)

	Date <u>2/27/03</u>
(print name) _____	
COMMENTS: _____	

## BUSINESS UNIT VP/GM APPROVAL: (required)

_____	Date _____
COMMENTS: _____	

On the following Invention Disclosure Sheet(s) describe the various aspects of the invention according to the following instructions:

1. **Background**: Describe the field to which invention relates, the most relevant prior art, and explain what is wrong with the prior art. Make sure to give adequate background information to enable the reader to clearly appreciate the problems that existed prior to your invention. Refer to and include relevant publications.
2. **Summary of Invention**: Briefly describe the present invention and how it solves the prior problem.
3. **Description of Invention**: Write a detailed description of the invention, referenced to sketches of the invention. If necessary, use additional sheets, and you may refer to separate drawings or photographs by number. The signature information at the bottom of this page must appear on each added sheet and on each separate drawing or photograph.
4. **Differences Over Known Prior Art**: Identify significant differences over any known prior art if possible.
5. **Advantages**: List and explain the advantages of the invention in the order of their importance.
6. **Witness**: Have two individuals, not inventors and co-inventors, read, understand, sign and date each Invention Disclosure Sheet.

# BROADCOM CORPORATION

Invention Disclosur Form (*cont'd*)

**CONFIDENTIAL**

## **INVENTION DISCLOSURE SHEET**

### High Voltage Power Management Unit Architecture in CMOS Process

Sheet 1 of 4

#### Background

Power Management Unit (PMU) is an important component in many applications such as cell phone, PDA, and any hand -held device. The function of Power Management Unit is to convert power-supply sources such as battery cells or battery chargers to suitable voltage levels for other components in the system. Since the operating voltage of power supply sources is usually higher than the breakdown voltage of standard CMOS technology, the PMU was implemented by technologies with high-voltage-breakdown devices such as Bipolar or non-standard CMOS. In this invention we propose a architecture for Power Management Unit that can be implemented in a low breakdown-voltage CMOS technology with low power consumption.

Signature of Inventor

2/27/03

Date

Signature of Inventor

2/27/03

Date

Signature of Inventor

Date

Signature of Inventor

Date

#### WITNESSED AND UNDERSTOOD:

Witness (Not an Inventor)

2/27/03

Date

Witness (Not an Inventor)

Date

## BROADCOM CORPORATION

Invention Disclosur Form (cont'd)

**CONFIDENTIAL**

### **INVENTION DISCLOSURE SHEET**

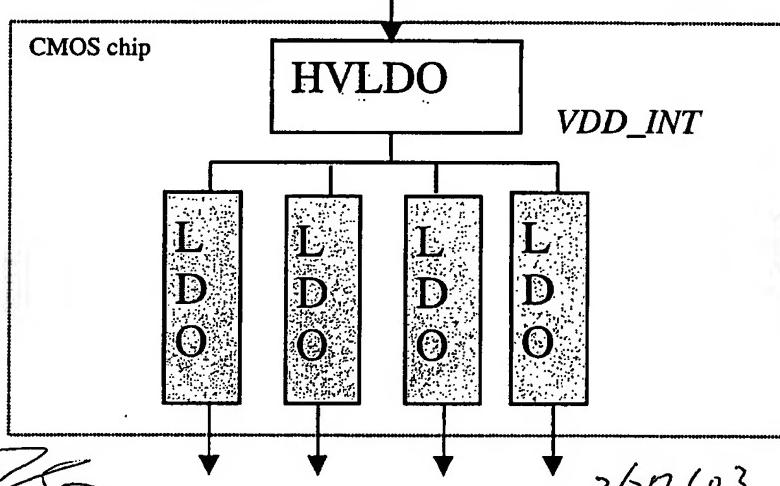
#### High Voltage Power Management Unit Architecture in CMOS Process

Sheet 2 of 4

#### Summary/Description of Invention

The Power Management Unit was implemented in two stages: First stage, called High Voltage Low Drop-Out regulator (HVLDO), regulates the high-voltage supply to the voltage (VDD\_INT) that the standard CMOS device can tolerate. The following stages, called Low Drop-Out regulators (LDO), regulate VDD\_INT to all suitable voltages to supply other components. The first stage consumes small power to maintain device not to exceed breakdown voltage. However, each regulate in the second stage can be powered down and can be implemented in low power design without consideration of device breakdown issues. Thus a very low power design can be achieved.

*External high voltage supply*



Signature of Inventor

Date

*[Signature]*

2/27/03

Signature of Inventor

Date

Signature of Inventor

Date

Signature of Inventor

Date

#### **WITNESSED AND UNDERSTOOD:**

*[Signature]*

2/27/03

Witness (Not an Inventor)

Date

Witness (Not an Inventor)

## BROADCOM CORPORATION

Invention Disclosur Form (*cont'd*)

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### ***INVENTION DISCLOSURE SHEET***

#### **High Voltage Power Management Unit Architecture in CMOS Process**

Sheet 3 of 4

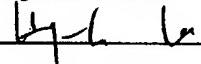
#### **Difference over Known Prior Art**

For other architecture such as single-stage architecture, each LDO regulates power directly from high-voltage supply down to lower voltages. Complex circuits and significant power consumption have to be paid in order to prevent device breakdown if the device breakdown voltage is lower than the supply voltage. Also, every LDO can not be completely powered down due to that breakdown issue, thus more power consumption in the power-off state.

  
\_\_\_\_\_  
Signature of Inventor

2/27/03

Date

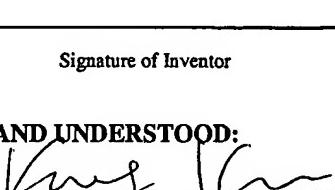
  
\_\_\_\_\_  
Signature of Inventor

2/27/03

Date

  
\_\_\_\_\_  
Signature of Inventor

Date

  
\_\_\_\_\_  
Signature of Inventor

2/27/03

Date

#### **WITNESSED AND UNDERSTOOD:**

  
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Witness (Not an Inventor)

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Witness (Not an Inventor)

# BROADCOM CORPORATION

Invention Disclosur Form (*cont'd*)

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## **INVENTION DISCLOSURE SHEET**

### High Voltage Power Management Unit Architecture in CMOS Process

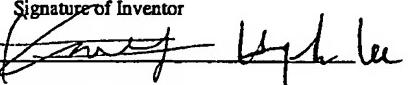
Sheet 4 of 4

#### **Advantages**

The advantage of using the two-stage architecture is low-power consumption. A single high voltage circuit stage is only needed to be implemented in the first stage. The second-stage LDOs do not require any breakdown prevention circuit and can be powered down in OFF mode. Thus less power consumption is achieved especially in the power-off state.

  
\_\_\_\_\_  
Signature of Inventor

2/27/03  
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Date

  
\_\_\_\_\_  
Signature of Inventor

2/27/03  
\_\_\_\_\_  
Date

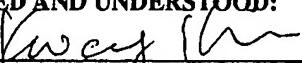
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Signature of Inventor

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Date

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Signature of Inventor

\_\_\_\_\_  
Date

#### **WITNESSED AND UNDERSTOQD:**

  
\_\_\_\_\_  
Witness (Not an Inventor)

2/27/03  
\_\_\_\_\_  
Date

\_\_\_\_\_  
Witness (Not an Inventor)

**From:** "Jeffrey Helvey" <JHELVEY@skgf.com>  
**To:** <cychen@broadcom.com>  
**Date:** 7/10/03 4:48PM  
**Subject:** Re: RE: preliminary draft application--voltage regulators (1875.4150000 )

CY,

Here is the first draft. Please review and provide George with any comments that you have.

Please be reminded that the duty of disclosure continues throughout the entire patent application process, and ends only with the actual issuance of a patent. Therefore, if anyone substantively involved in the patent application process becomes aware of information that might be considered material, please forward it to us immediately.

Thanks,  
Jeff Helvey  
Sterne, Kessler, Goldstein, & Fox  
1100 New York Ave, NW  
Washington DC, 20005  
(202)772-8675 (voice)  
(202)371-2540 (fax)  
jhelvey@skgf.com

>>> George Bardmesser 07/10/03 07:25AM >>>

CY, sorry for the delay--I am out of the country right now, but Jeff Helvey has it for review. We will get it to you in the next few days.

Again, sorry about the delay.

>>> "Chun-Ying Chen" <cychen@broadcom.com> 07/09/03 15:01 PM >>>

George:  
How's the status of the three PMU related patent application?

Thanks,

CY

-----Original Message-----

From: Chun-Ying Chen [mailto:cychen@broadcom.com]  
Sent: Tuesday, May 20, 2003 4:46 PM  
To: George Bardmesser  
Subject: RE: preliminary draft application--voltage regulators  
(1875.4150000 )

George:  
I am available for tomorrow. Just give me a call when you have time.  
Thanks,

CY

-----Original Message-----

From: George Bardmesser [mailto:GBARDMES@skgf.com]  
Sent: Tuesday, May 20, 2003 1:51 PM

To: cychen@broadcom.com  
Subject: preliminary draft application--voltage regulators (1875.4150000 )

<< File: ATT00085.txt >> << File: 127498\_1.doc >> << File:  
Visio-0302-01.pdf >> Hi CY--

this is still a very preliminary draft (notice, e.g., there is no FIG. 10, and not that many claims), but I would appreciate it if you could look it over, and make sure that I am on the right track.

I am flying to the Middle East on business tomorrow night, so if we could discuss it tomorrow, that would be great. Otherwise, we can do it next week sometime.

Best regards,

George.

George S. Bardmesser  
Sterne Kessler Goldstein & Fox  
1100 New York Avenue, N.W.  
Washington, DC 20005  
Email: [gbardmes@skgf.com](mailto:gbardmes@skgf.com)  
Phone: 202-772-8782  
Fax: 202-371-2540  
Cellular: 301-802-7605

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CC: "George Bardmesser" <[GBARDMES@skgf.com](mailto:GBARDMES@skgf.com)>